storage means for holding a predetermined number N of individual instructions, including at least one group of M individual instructions to be executed in parallel, where $M \leq N$, each individual instruction in the storage means having associated therewith a pipeline identifier indicative of the processing pipeline for executing that individual instruction and a group identifier indicative of the group of individual instructions to [be executed] which it is assigned for execution in parallel;

group decoder means responsive to the group identifier for causing all individual instructions having the same group identifier to be executed [at the same time] in parallel; and

pipeline decoder means responsive to the pipeline identifier of the individual instructions in the group [to supply] for causing each individual instruction in the group [to be executed in parallel] to be supplied to an appropriate processing pipeline.

2. (Amended) A computing system as in claim 1 wherein the storage means includes the at least one group of individual instructions, and for each individual instruction the storage means also includes the group identifier and the pipeline identifier.

3. (Amended) A computing system as in claim 2 wherein each individual instruction in the at least one group of individual instructions has associated therewith a different pipeline identifier.

4. (Amended) A computing system as in claim 1 wherein the storage means holds [at least two groups of instructions, and] a first group of individual instructions to be executed in parallel and a second group of individual instructions to be executed in parallel after the first

group, [all of] the individual instructions in each group having associated therewith a common group identifier [are] being placed adjacent to each other in the storage means.

5. (Amended) A computing system as in claim 4 wherein:

the storage means comprises a line in a cache memory having a fixed number of storage locations;

the first group of individual instructions [to be executed first] is placed at one end of the line in the cache memory, and the second group of individual instructions [in the group] to be executed [last] next is placed [at the other end of the line in the cache memory] next to the first group of individual instructions.

6. (Amended) A method of executing arbitrary numbers of instructions in a stream of instructions in parallel which have been compiled to determine which instructions can be executed [at the same time,] in parallel, the method comprising:

in response to the compilation, assigning a common group identifier[s] to [sets] a group of instructions which can be executed in parallel;

determining a processing pipeline for execution of each instruction in [a] the group [to be executed;] of instructions to be executed;

assigning a pipeline identifier to each instruction in the group; and

placing a fixed number of the instructions in a register, which number includes at least one group of instructions having the common group identifier as well as at least one other instruction having a different group identifier [for execution by the pipelines].

7. (Amended) A method as in claim 6 further comprising the step of executing [a] the group of instructions in parallel.

8. (Amended) A method as in claim 7 wherein the register holds at least two groups of instructions, and the step of placing the instructions in the register for execution by the processing pipelines comprises placing the instructions in each group having associated therewith a common group identifier adjacent to each other in the register.

9. (Amended) A method as in claim 8 wherein the step of executing a group of instructions in parallel comprises coupling the register to detection means to receive the group identifier of each instruction in the register and the group identifier of the next group of instructions to be supplied to the processing pipelines; and

supplying only the instructions with the next group identifier to the processing pipelines. [execution units.]

10. (Amended) In a computing system in which a group[s] of individual instructions are executable in parallel by processing pipelines, a method for supplying each individual instruction in [a] the group to be executed in parallel to [an] corresponding appropriate processing pipelines, the method comprising:

storing in storage an instruction frame, the frame including at least one group of individual instructions to be executed in parallel, each individual instruction in the group having associated therewith a pipeline identifier indicative of the processing pipeline which will execute that instruction and a group identifier indicative of the group identification;

comparing the group identifier of each individual instruction in the instruction frame [and a group] with an execution identifier of those instructions to be next executed [in parallel]; and

using the pipeline identifier of those individual instructions to be next executed [in parallel to control an execution unit] to execute [all] each of the individual instructions in the group in separate processing pipelines.

11. (Amended) In a computing system in which groups of individual instructions are executable in parallel by a set of processing pipelines, apparatus for routing each instruction in a group to be executed in parallel to an appropriate processing pipeline, the apparatus comprising:

storage for holding at least one group of instructions to be executed in parallel, each instruction in the group having associated therewith a pipeline identifier indicative of the processing pipeline for executing that instruction and a group identifier to designate among the instructions present in the storage those instructions which may be simultaneously supplied to the processing pipelines.

a crossbar switch having a first set of connectors coupled to the storage for [receiving] transferring instructions therefrom [and] to a second set of connectors coupled to the processing pipelines;

[means] a router responsive to the pipeline identifier of the individual instructions in the group for routing individual instructions onto appropriate ones of the second set of connectors, to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.

12. Apparatus as in claim 11 wherein:

the first set of connectors [consists of] includes a set of first communication buses, one for each instruction in the storage;

the second set of connectors [consists of] includes a set of second communication buses, one for each processing pipeline; and

[the means] the router responsive to the pipeline identifier comprises:

a set of decoders coupled to the storage, each decoder to receive as a first input signal[s] the pipeline identifier[s] of a corresponding instruction in the storage and in response thereto supply as output signals [a] corresponding switch control signals; and

a set of switches, coupled to the decoders to receive the switch control signals, one switch at the intersection of each of the first set of connectors with each of the second set of connectors, the switches providing connections in response to receiving the corresponding switch control signal to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.

13. (Amended) Apparatus as in claim 12 further comprising:

detection means coupled to receive the group identifier of each instruction in the storage and connected to receive information regarding [the group identifier of] the next group of instructions to be supplied to the processing pipelines, and in response thereto supply a group control signal; and

wherein the set of decoders coupled to the storage are also coupled to the detection means to receive the group control signal and in response thereto [supplies] supply a switch control signal for only those instructions in the group to be supplied to the processing pipelines.

14. (Amended) Apparatus as in claim 13 wherein the detection means comprises a multiplexer coupled to receive [each of] the group identifier[s] of <u>each</u> instruction[s] in the storage <u>and the group identifier of the next group of instructions to be executed,</u> and<u>, in response allow</u> [compare them to the information regarding the group identifier of] the next group of instructions to be supplied to the <u>processing</u> pipelines.

15. (Amended) Apparatus as in claim 14 wherein the multiplexer supplies an output signal to the decoders to indicate the group identifier of the next group of instructions to be supplied to the <u>processing</u> pipelines.

16. (Amended) In a computing system in which <u>a</u> group[s] of individual instructions are executable in parallel by processing pipelines, apparatus for routing each instruction in a group to be executed in parallel to an appropriate <u>processing</u> pipeline, the apparatus comprising:

a storage for holding an instruction frame, the frame including at least one group of instructions to be executed in parallel, each instruction in the group having associated therewith a pipeline identifier indicative of the <u>processing</u> pipeline to which that instruction is to be issued and a group identifier indicative of the group [identification];

a crossbar switch having a first set of connectors coupled to the storage for receiving instructions therefrom and a second set of connectors coupled to the processing pipelines;

selection means connected to receive the group identification of each instruction in the instruction frame and connected to receive information about the group identifier of those instructions to be next executed [in parallel] for supplying in response thereto [an output

signal indicative of] a control signal to permit the next [set] group of instructions to be executed in parallel; and

decoder means coupled to the selection means to receive the [output] control signal and each of the pipeline identifiers of the instructions in the storage for selectively connecting ones of the first set of connectors to ones of the second set of connectors to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.

17. (Amended) Apparatus as in claim 16 wherein the first set of connectors consists of a set of first communication buses, one for each instruction in the storage;

the second set of connectors consists of a set of second communication buses, one for each processing pipeline;

the decoder means comprises a set of decoders coupled to receive as first input signals the pipeline identifiers and as second input signals information about the group identifier of the next group of instructions to be executed by the pipelines and in response thereto supply [as output signals a] corresponding switch control signals; and

the crossbar switch includes a set of switches, one at the intersection of each of the first set of connectors with the second set of connectors, the switches providing connections in response to receiving the switch control signals to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.

18. (Amended) Apparatus as in claim 17 wherein the selection means coupled to the storage comprises a multiplexer coupled to receive each of the group identifiers of instructions in the storage, and [compare them] in

response to information regarding the group identifier of the next group of instructions to be supplied to the pipelines, enable appropriate instructions to be supplied to the processing pipelines.

19. (Amended) Apparatus as in claim 18 wherein the multiplexer supplies an output signal to the decoders to select the group identifier of the next group of instructions to be supplied to the processing pipelines.

20. (Amended) In a computing system in which a group[s] of individual instructions are executable in parallel by processing pipelines, a method for transferring each instruction in a group to be executed through a crossbar switch having a first set of connectors coupled to the storage for receiving instructions therefrom and a second set of connectors coupled to the processing pipelines, the method comprising:

storing in storage a set of instructions including at least one group of instructions to be executed in parallel, each instruction in the group having associated therewith a unique pipeline identifier indicative of the processing pipeline which will execute that instruction, and also including at least one other instruction not in the at least one group of instructions, which other instruction also having associated therewith a pipeline identifier; and

using the pipeline identifiers of the individual instructions in the at least one group of instructions which are to be executed next to control switches between the first set of connectors and the second set of connectors to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.

21. A method as in claim 20 wherein the step of using the pipeline identifiers comprises:

supplying the pipeline identifiers of the individual instructions in the at least one group of instructions to [a corresponding number of decoders,] individual ones of a set of decoders, each of which provides an output signal indicative of the pipeline identifiers of the individual instruction supplied thereto; and

using the decoder output signals to control the switches between the first set of connectors and the second set of connectors to thereby supply each individual instruction in the group to be executed in parallel to [the] an appropriate processing pipeline.

22. (Amended) A method as in claim 21 wherein each of the individual instructions in the storage further includes a group identifier to designate among the instructions present in the storage which may be simultaneously supplied to the processing pipelines, and the method further comprises:

supplying information about the group identifier of the next group of instructions to be executed by the processing pipelines together with the group identifiers of the individual instructions in the at least one group of instructions to a selector;

comparing the group identifier of the next group of instructions to be executed by the processing pipelines with the group identifiers of the individual instructions in the at least one group of instructions, to provide output comparison signals; and

using both the output comparison signals and the decoder output signals to control the switches [be tween] between the first set of connectors and the second set of connectors to thereby supply each instruction in the group to be executed in parallel to the appropriate processing pipeline.